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JUL 10 2007

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented) A method comprising:

determining whether execution of an instruction of a first thread executed in a processor potentially causes a long latency based on whether the instruction hits in a lookup table in an instruction decoder of the processor, the lookup table including entries corresponding to predetermined conditions;

preparing to switch to a second thread based on the determination by selecting a program counter of the second thread within an instruction fetch unit of the processor to fetch a next instruction of the second thread, and executing at least one additional instruction in the first thread present in a pipeline of the processor and storing a result of the at least one additional instruction in a destination storage instead of flushing the at least one addition instruction while preparing to switch to the second thread; and

switching to the second thread if the potential long latency is determined, executing one or more instructions of the second thread in the processor, and storing a result of the one or more instructions of the second thread in the processor.

Claim 2 (canceled)

Claim 3 (previously presented) The method of claim 1, wherein the determining is based on a stochastic modeling of whether the instruction will result in a long latency.

Claim 4 (canceled)

Claim 5 (previously presented) The method of claim 1, further comprising providing a feedback signal from the instruction decoder to the instruction fetch unit to switch to the second thread if the instruction matches an entry in the lookup table.

Claim 6 (original) The method of claim 1, wherein the long latency comprises less than ten processor cycles.

Claim 7 (canceled)

Claims 8 – 16 (canceled)

Claims 17 – 24 (cancel)

Claim 25 (canceled)

Claims 26-29 (cancel)

Claim 30 (previously presented) The method of claim 1, wherein the predetermined conditions comprise instruction types.

Claim 31 (canceled)

Claim 32 (previously presented): The method of claim 5, further comprising executing two instructions of the first thread while preparing to switch to the second thread, wherein the feedback signal has a two pipeline stage delay.